REMARKS

In response to the Office Action dated May 10, 2010 Applicant respectfully requests reconsideration based on the above claim amendments and the following remarks. Applicant respectfully submits that the claims as presented are in condition for allowance.

Claims 1-11 and 14-17 are pending in the present Application. Claims 1 and 7 are amended, leaving Claims 1-11 and 14-17 for consideration upon entry of the present amendments and the following remarks.

Support for the claim amendments is at least found in the specification, the figures, and the claims as originally filed. Particularly, support for amended Claims 1 and 7 is at least found in originally filed Figures 4 and 6, and in the specification at page 10, line 20 to page 11, line 10, and, page 13, lines 4-23.

No new matter has been introduced by these amendments. Reconsideration and allowance of the claims are respectfully requested in view of the above amendments and the following remarks.

Claim Rejections under 35 U.S.C. §103

Claims 1-6, 7-11 and 14-17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kawaguchi et al., U.S. Patent No. 5,592,199 (hereinafter "Kawaguchi"), in view of Nakamura et al., U.S. Patent No. 7,136,058 (hereinafter "Nakamura"), and further in view of McCartney, U.S. Patent No. 6,497,022 (hereinafter "McCartney".

Applicant respectfully traverses the rejections for the reasons set forth below.

In a conventional LCD apparatus illustrated in Figure 1 and described at page 4, lines 10-13 and lines 18-21:

> As shown in FIG. 1, the output instruction signal line 180 that provides the output instruction signal TP to the data driving chip 160 is formed on the data PCB 120, so that the output instruction signal line 180 does not have the capacitive load as that of the gate lines GL.
>
> Therefore, in the conventional LCD apparatus, a waveform of the data signal is not equal to a waveform of the gate driving signal. As a result, the gate driving signal may not be applied to the gate lines GL while the data signal is applied to the corresponding data lines DL, thereby an abnormal image displayed on the display screen of the LCD apparatus.

A non-limiting embodiment of the invention described at page 10, line 20 to page 11, line 10:

> As described above, since the output instruction signal line 510 used as a path of the output instruction signal TP is formed on the TFT substrate 414, which is substantially parallel to the gate lines GL, the output instruction signal line 510 has the capacitive load and resistive load substantially same as those of the gate lines GL.
>
> That is, **the output instruction signal line 510 has the capacitive load because the output instruction signal line 510 acts as a capacitor with the common electrode (not shown) formed on the color filter substrate 416**. Also, the output instruction signal line 510 also has the resistive load because the output instruction signal line 510 acting as one of resistors.
>
> Thus, the output instruction signal TP provided to the data driving chip 440 via the output instruction signal line 510 may be delayed due to the capacitive and resistive loads of the output instruction signal line 510.
>
> Particularly, when the output instruction signal TP is provided to the driving chip 440 via a relatively-long output instruction signal line TP, the output instruction signal TP may be more delayed than when the output instruction signal TP is provided to the driving chip 440 via a relatively-short output instruction signal line TP. In this case, a delayed-time of the output instruction signal TP is substantially equal to a delayed-time of the gate driving signal.

In the claimed invention, since the instruction signal line opposes the common electrode, and the capacitive load of the output instruction signal line is defined solely by the output instruction signal line acting as a capacitor with the common electrode,

independent **Claims 1 and 7** are hereinabove amended to similarly recite, *inter alia*:

"*an output instruction signal line disposed on the second substrate and opposing the common electrode*; and

a timing controller providing a first control signal to the gate driver so as to control an output of the gate driving signal, and providing an output instruction signal to the data driver via the output instruction signal line *to delay the output instruction signal depending on a capacitive load solely defined by the output instruction signal line opposing the common* electrode, and depending on a resistive load of the output instruction signal line,

wherein the data driver outputs a delayed image data signal to the LCD panel as the output instruction signal is delayed *such that a delayed time of the image signal is substantially equal to a delayed time of the gate driving signal*."

Regarding **Kawaguchi** in the instant Office action at Pages 4, 5 and 7-9, common lines 231, flexible wiring boards 230 along y-axis with six drive IC's 229, and connector 8/control board 232 (Figure 1, Col. 19, lines 15-18/Figure 30, Col. 28, lines 6-14) in Figures 30-32 of Kawaguchi are respectively considered as teaching the "output instruction signal line," the "data TCP," and the "timing controller" of independent Claims 1 and 7. It is conceded on Page 4 of the instant Office action that Kawaguchi does not expressly teach 1) a common electrode disposed on the first substrate or that the output instruction signal line opposes the common

electrode. It is further conceded on Page 5 of the instant Office action that Kawaguchi does not expressly teach 2) a delayed time of the image signal is substantially equal to a delayed time of the gate driving signal.

Regarding **Nakamura** in the instant Office action with respect to independent Claims 1 and 7 at Pages 4 and 5, Nakamura is relied upon as allegedly teaching a common electrode disposed on the first substrate and opposing a "signal line." Specifically, Col. 4, lines 10-19, *power supply* wiring pattern P1 and *capacitor* elements C4,C5 wiring in Figures 14 and 15 of Nakamura are relied upon as teaching "signal lines" disposed on the second substrate and opposing the common electrode.

In a telephone interview completed on August 4, 2010 between the Examiner of record and Applicant's undersigned attorney, it was further explained by the Examiner that Nakamura is being used to evidence the desirability of locating "lines" other than those conventionally opposing the common electrode, e.g., gate and data lines, opposite to a common electrode, as motivated by, for example, a reduction in the frame size of the LCD, resulting in a more portable display, as described in Col. 15, lines 42-50 of Nakamura.

Regarding **McCartney** in the instant Office action at Page 5, column driver circuits CD1-10 (reference numerals 70-80) are considered as teaching the "data driver" outputting a delayed image data signal (output of 70-80 in Figure 5) to display panel as the *output instruction signal line* (IN in Figure 5) is delayed such that a delayed time of the image signal is substantially equal to a delayed time of the gate driving signal, as evidenced by Col. 6, lines 59-66. It is then asserted on Page 5 of the instant Office action that it would have been obvious to one of ordinary skill in the art to include the circuitry of McCartney to ensure that the image signal is equal to the delayed time of the gate driving signal.

In a telephone interview completed on August 4, 2010 between the Examiner of record and Applicant's undersigned attorney, it was further explained by the Examiner that the teaching of a delay for the column driver enable signal which approximates the delay experienced by a row enable signal of McCartney, is being used to evidence "the output instruction signal is delayed such that a delayed time of the image signal is *substantially equal to a delayed time of the gate driving signal*" of the claimed invention.

As discussed above, common lines 231 of **Kawaguchi** are considered as teaching the "output instruction signal line." It is asserted on Page 4 of the instant Office action that the resistive load attributed to the metallic signal line which provides the "output instruction signal" in Kawaguchi will *inherently* cause delay and each data driver in Figure 30 of Kawaguchi will be *at least slightly delayed* in outputting the data signal. As discussed above, Kawaguchi does not expressly teach 1) a common electrode disposed on the first substrate or that the output instruction signal line opposes the common electrode, and 2) a delayed time of the image signal is substantially equal to a delayed time of the gate driving signal.

That is, Kawaguchi does not teach or suggest creating a capacitor between a common electrode and the common lines 231, such that a delayed time of the image signal is *substantially equal to a delayed time of the gate driving signal*" as recited in independent Claims 1 and 7.

Nakamura teaches signal lines through which an amplified and D/A converted analog *video signal* passes. (See, for example, Col. 4, lines 10-11 and 21-24.) Nakamura teaches *power supply wiring* pattern P1 of AMP 17 which amplifies an output from the DAC 16, overlaps common electrode 23. (See, Col. 15, lines 43-48.) Nakamura further teaches *capacitor* elements C4 and C5 are connected between stages of inverters IV1 to IV 3 *in the AMP 17*. (See, Col. 15, lines 51-55 and Figure 15.)

That is, Nakamura does not teach or suggest creating a capacitor between the common electrode and a signal line (e.g., the power wiring pattern P1), such that a delayed time of the image signal is *substantially equal to a delayed time of the gate driving signal*" as recited in independent Claims 1 and 7.

McCartney teaches to create delay for the column driver enable signal which approximates the delay experienced by a row enable signal, a plurality of resistive and capacitive elements 68 and 68 are coupled in a delay line as shown in Figure 5. (See, Col. 6, lines 62-66 and Figure 5 of McCartney.) Applicant finds no teaching or suggestion of the delay line of McCartney relative to a common electrode, such as included in the display panel. That is, similar to Kawaguchi, McCartney also does not teach a common electrode disposed on the first substrate or the delay line opposing the common electrode, such that the delay for the column driver enable signal which approximates the delay experienced by a row enable signal, e.g., a

delayed time of the image signal is substantially equal to a delayed time of the gate driving signal.

Specifically, McCartney teaches the delay imposed on the column driver enable signal used for each column driver circuit 70-80 is chosen to approximate the delay needed for the first column signal line amount that group of column signal lines. (See, Col. 7, lines 14-17 of McCartney.) McCartney teaches at Col. 7, line 17-59, a graph is used to divide a delay curve by the number of column driver circuits, and then implementing the resulting delay. That is, the delay in the delay line IN of McCartney is *not due to a resistive load relative to a common electrode*, contrary to the claimed invention.

That is, McCartney does not teach or suggest creating a capacitor between a common electrode and the delay line, such that a delayed time of the image signal is *substantially equal to a delayed time of the gate driving signal*" as recited in independent Claims 1 and 7.

Therefore, Kawaguchi, Nakamura and McCartney, alone or in combination, *fail to teach or suggest* **an output instruction signal line disposed on the second substrate and opposing the common electrode**, and a timing controller providing an output instruction signal to the data driver **via the output instruction signal line to delay the output instruction signal depending on a capacitive load solely defined by the output instruction signal line opposing the common electrode**, and depending on a resistive load of the output instruction signal line, wherein the data driver outputs a delayed image data signal to the LCD panel as the output instruction signal is delayed **such that a delayed time of the image signal is substantially equal to a delayed time of the gate driving signal** of amended independent Claims 1 and 7.

Thus, since Kawaguchi, Nakamura and McCartney, alone or in combination, *fail to teach or suggest all of the limitations* of similarly amended independent Claims 1 and 7, *prima facie* obviousness does not exist regarding at least amended independent Claims 1 and 7 with respect to Kawaguchi, Nakamura and McCartney. Applicant respectfully submits that Claims 1 and 7, and Claims 2-6, 8-11 and 14-17 as respectively depending from Claims 1 and 7, are not further rejected or objected, and are therefore allowable. Entry of the claim amendments, reconsideration, withdrawal of the relevant §103 rejections and allowance of Claims 1-11 and 14-17 are respectfully requested.

Conclusion

All of the objections and rejections are herein overcome. In view of the foregoing, it is respectfully submitted that the instant application is in condition for allowance. No new matter is added by way of the present Amendments and Remarks, as support is found throughout the original filed specification, claims and drawings. Prompt issuance of Notice of Allowance is respectfully requested.

The Examiner is invited to contact Applicant's attorney at the below listed phone number regarding this response or otherwise concerning the present application.

Applicant hereby petitions for any necessary extension of time required under 37 C.F.R. 1.136(a) or 1.136(b) which may be required for entry and consideration of the present Reply.

If there are any charges due with respect to this Amendment or otherwise, please charge them to Deposit Account No. 06-1130 maintained by Applicant's attorneys.

Respectfully submitted,

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